Hybrid CMOS / Nanoelectronic Circuits: Prospects and Challenges

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I will review the recent work on devices, circuits and architectures for hybrid semiconductor/ nanodevice integrated circuits based on nanowire crossbars, with similar, simple, two-terminal devices (with the functionality of programmable diodes) formed at each crosspoint. Special attention will be given to the so-called "CMOL" variety of the hybrids, in which the crossbar is connected to the underlying CMOS circuit with an area-distributed interface. Such interface allows the CMOS subsystem to address each and every of the crosspoint devices, even with no nanoscale alignment between the CMOS and crossbar subsystems. The recent detailed studies have shown CMOL may enable (at least) the following applications:

(i) terabit-scale memories with access time below 100 ns and defect tolerance up to 10%,
(ii) FPGA-like reconfigurable logic circuits with the area-by-delay product at least two orders of magnitude lower than that of CMOS FPGAs fabricated with similar design rules and power per unit area, and
(iii) mixed-signal neuromorphic networks ("CrossNets") which may provide unparalleled performance for some important information processing tasks, and in future may become the first hardware basis for challenging the human cerebral cortex in both density and speed.

Recently, the hybrid circuit concept has received a strong boost from the experimental demonstrations of reproducible crosspoint devices (programmable diodes) based on metal oxides and amorphous silicon, and nanowire crossbars with 15-nm-scale half-pitch. However, the transfer of semiconductor IC industry to the hybrid technology will still require a very substantial effort, and I will describe the most significant challenges on that way.

Links to publications may be found online at
http://rsfq1.physics.sunysb.edu/~likharev/nano/ .